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Resistive switching in zinc–tin-oxide

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ABSTRACT

Bipolar resistive switching is demonstrated in the amorphous oxide semiconductor zinc–tin-oxide (ZTO). A gradual forming process produces improved switching uniformity. Al/ZTO/Pt crossbar devices show switching ratios greater than 10^3, long retention times, and good endurance. The resistive switching in these devices is consistent with a combined filamentary/interfacial mechanism. Overall, ZTO shows great potential as a low cost material for embedding memristive memory with thin film transistor logic for large area electronics.

1. Introduction

Resistive random access memories (RRAMs), also known as memristors, are being considered as a potential next-generation replacement for non-volatile flash memory due to their simple structure and potential for rapid program/erase speed, high areal density, and low power consumption [1–14]. Thin film transistors (TFTs) based on transparent wide bandgap amorphous oxide semiconductors such as indium–gallium–zinc-oxide (IGZO) [15] and zinc–tin-oxide (ZTO) [16,17] are rapidly approaching commercialization as a replacement for amorphous Si in high performance large area electronics (macroelectronics) applications such as liquid crystal displays (LCDs). Both IGZO and ZTO have good electron mobility, show good TFT performance and have high transparency. Recently resistive switching has been reported in IGZO [10,11], opening the possibility of large area transparent electronics with embedded transparent memory.

In this article, we demonstrate bipolar resistive switching (BRS) using solution deposited amorphous ZTO as the active switching material. A significant advantage of ZTO over IGZO is that ZTO does not contain In or Ga, two elements which are becoming increasingly expensive and potentially scarce. The impact of the compliance current (CC) magnitude on the switching uniformity, the switching ratio, the retention, and the endurance is investigated with respect to device area. We find that a gradual-forming (GF) process, in which the CC on the initial SET operation is gradually increased until the first bipolar RESET operation is observed, improves the switching uniformity. Resistive switching in these Al/ZTO/Pt devices is consistent with a combined filamentary/interfacial model.

2. Materials and methods

The ZTO active switching layer was formed via solution based chemistries that have been previously used for TFTs [17]. Zinc chloride ($ZnCl_2$) and tin chloride ($SnCl_2$) precursors were dissolved in a mixture of acetonitrile and ethyleneglycol with a 1:1 volume ratio and then spin coated to form a uniform continuous film. The films were dried at 100 °C and then annealed for 2 h at 500 °C in air. This annealing process completes the conversion to a metal oxide ZTO film. ZTO was patterned using SU-8 photoresist and etched using 0.1 M oxalic acid. The lack of long range crystalline order in ZTO thin films formed using this method has been demonstrated previously using X-ray diffraction [17]. ZTO film thickness was determined using a J.A. Woolam spectroscopic ellipsometer and a Cauchy model.

Standard metal–insulator–metal (MIM) crossbar devices ranging in area from 10 μm × 10 μm to 100 μm × 100 μm were fabricated on Si substrates with an SiO_2 insulating layer using Pt as a

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bottom electrode and Al as the top electrode. The 50 nm thick Pt bottom electrode was deposited via e-beam evaporation using a 25 nm layer of Ti as an adhesion layer. The Al top electrode was deposited via thermal evaporation. Both Pt and Al were patterned via liftoff. Electrical characterization was performed in the dark at room temperature using an Agilent 4155 semiconductor parameter analyzer and a probe station.

3. Results and discussion

Shown in Fig. 1a are a series of resistance switching cycles for a 50 μm × 50 μm Al/ZTO/Pt MIM device with a 6 nm thick layer of ZTO. For clarity, complete sweeps are not shown. All biases are applied to the Al top electrode with the Pt bottom electrode held at ground. Although ZTO MIM devices are initially in a high resistance state (HRS), a distinct forming process, in which a much higher initial SET voltage is needed to begin the switching process, is not required. (The SET operation is defined as switching from the HRS to the low resistance state (LRS); the RESET operation as switching from the LRS back to the HRS.) A CC of 150 μA is used to prevent permanent dielectric breakdown of the ZTO during the SET operations. Although BRS is observed, large variation in the SET current (I_{SET}), the RESET current (I_{RESET}), the SET voltage (V_{SET}), and the RESET voltage (V_{RESET}) occur.

It was found that device operation could be improved greatly with a gradual forming (GF) process. Shown in Fig. 1b is a similar 50 μm × 50 μm device with an identical operating CC of 150 μA that received the GF procedure. The GF procedure involves sequentially increasing the CC on the initial negative bias SET operation until the LRS and the first bipolar RESET operation is observed at positive bias. In brief, the CC during the initial SET sweep on a fresh device is fixed at a low value (50 nA in Fig. 1b) and the top Al contact bias is swept negative until an abrupt increase in current is observed. The device is then checked with a positive bias sweep to determine whether it is in the LRS. If the LRS is not observed at positive bias, the CC is increased incrementally and the process is repeated until the LRS is detected at positive bias and the first bipolar switching event is observed. A CC of 250 nA in Fig. 1b is seen to be the lowest SET CC required to enable a bipolar switch at positive bias. This CC is defined to be the GF CC and is typically found to be in the 100s of nA range, independent of device area from 10^2 μm^2 to 10^4 μm^2. The relative independence of the GF CC on area is consistent with a conductive filament (CF) model. As seen in Fig. 1b, post-RESET current ($I_{post\text{-}RESET}$) and the corresponding I_{SET} are comparable to or greater than the GF CC. Therefore, a higher operating CC must be used and is chosen to minimize switching variability (high enough so that switching is repeatable, but low enough to prevent permanent hard breakdown of the device [18]). Although current overshoot due to parasitic capacitance is a possible explanation [19], a similar lack of dependence of I_{RESET} on the CC has been reported recently for HfO_2 based devices with a reactive top electrode [20]. Comparing Fig. 1b with Fig. 1a, it is seen that the GF process allows for greatly improved switching uniformity. Although the mechanism for this improvement is under investigation, one possible explanation is that the GF process assists in establishing the formation of simply connected CFs, rather than complex CFs (as discussed in [18] for RS in CoO). This reduces subsequent switching variability and also allows the HRS to be dominated by bulk conduction or a multitude of weak non-switching CFs [21].

A typical complete bipolar switching cycle for a 10 μm by 10 μm device with a gradual form CC = 500 nA is shown in Fig. 2. I_{SET}, V_{SET}, I_{RESET}, and V_{RESET} are labeled. We have found that bipolar switching only occurred when the initial SET operation has a negative bias applied to the Al electrode. Bipolar switching was not observed with an initial positive voltage sweep. RESET switching was not observed at negative bias. Note that the observed direction (or polarity dependence) of the RS is opposite to the direction of switching that is typically reported for devices with non-reactive

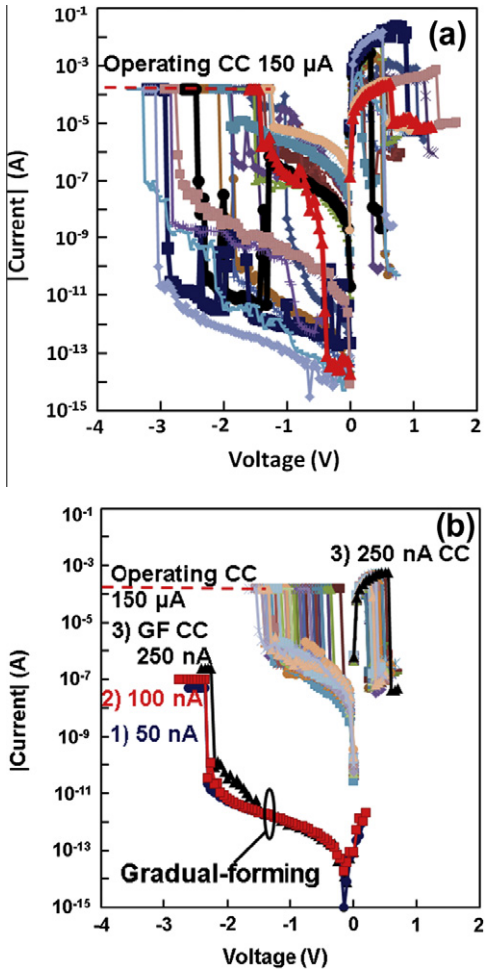

Fig. 1. Plot of log |current| vs. top electrode voltage for a 50 μm × 50 μm device with an operating CC of 150 μA (a) without the GF process and (b) with a GF CC of 250 nA.

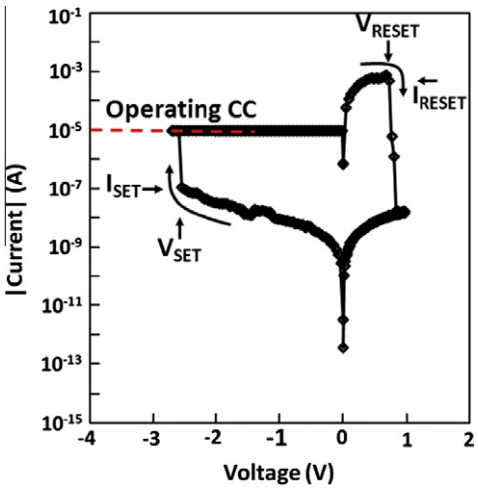

Fig. 2. Plot of log |current| vs. top electrode voltage showing a typical complete bipolar switching cycle for a 10 μm by 10 μm device with a gradual form CC of 500 nA.

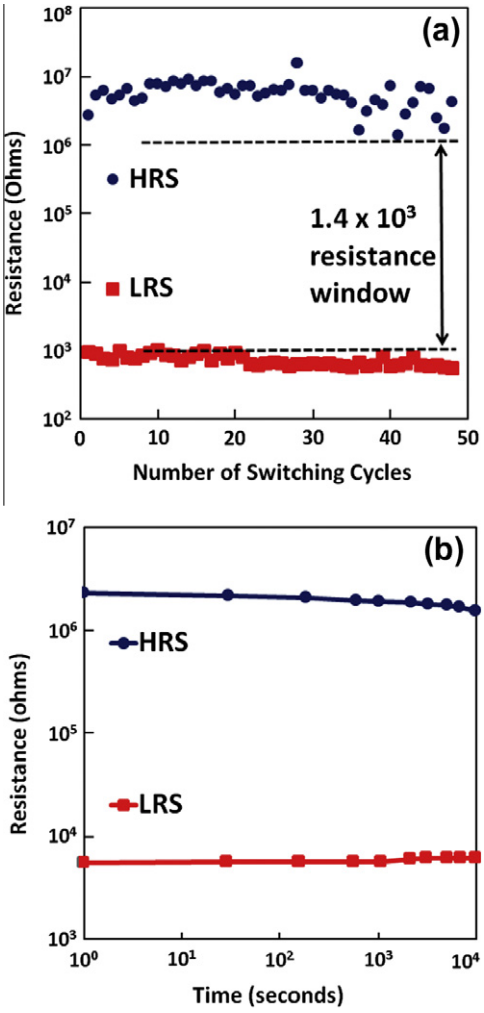

Fig. 3. R_{HRS} and R_{LRS} vs. (a) the number of switching cycles for the device from Fig. 1(b) and (b) vs. time for a similar device.

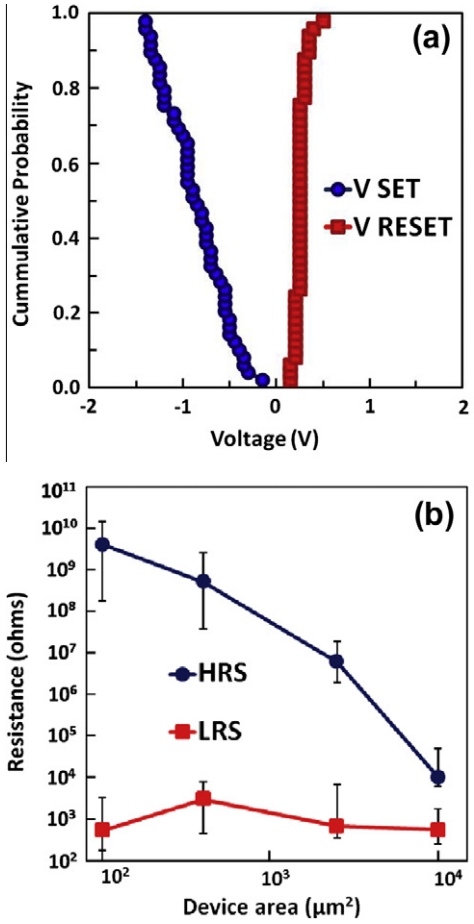

Fig. 4. (a) Cumulative probability plot of V_{SET} and V_{RESET} for a 50 μm × 50 μm device with gradual forming and an operating-CC of 150 μA. (b) Plot of the median HRS and LRS vs. device area (error bars indicate minimum and maximum values).

gates [8]. However, it is consistent with that reported for TiO_2 [5,22], ZnO [7], and $La_{0.7}Ca_{0.3}MnO_3$ [23] memristors with reactive Al top gate electrodes and suggests a role for an interfacial layer (IL) at the Al/ZTO interface. Note that the formation of an AlO_x layer at the Al/ZTO interface is thermodynamically favorable as indicated by the approximate Gibbs free energies of formation of the relevant oxides: $\Delta G^{\circ}_{Al2O3} = -1050$ kJ/mol, $\Delta G^{\circ}_{zno} = -625$ kJ/mol, $\Delta G^{\circ}_{sno} = -510$ kJ/mol, and $\Delta G^{\circ}_{sno2} = -515$ kJ/mol [24].

Shown in Fig. 3a is an endurance plot of the HRS resistance (R_{HRS}) and the LRS resistance (R_{LRS}) vs. the number of bipolar switching cycles for the device from Fig. 1b. The greater scatter in the R_{HRS} is commonly reported [8,25]. Although the switching endurance of these devices does not yet approach that of the leading materials [14], the observed minimum resistance window of approximately 1.4×10^3 is much larger than what is typically reported [14] and is more than sufficient for memory applications [2].

A retention plot of R_{HRS} and R_{LRS} vs. time is shown in Fig. 3b. After the GF was completed, the device was SET to the LRS at a negative voltage using an operating CC of 150 μA. The R_{LRS} was then measured periodically at 0.1 V for 10^4 s, after which the device was RESET under a positive voltage and the R_{HRS} was measured at −0.1 V periodically for another 10^4 s. Although the R_{HRS}/R_{LRS} ratio is still greater than 100 × after 10^4 s, it appears that some degradation of the memory window has occurred. The mechanism for this degradation is under investigation and work is underway to improve retention as well as endurance. Yang et al. [23] were able to improve the endurance of their Al/$La_{0.7}Ca_{0.3}MnO_3$/Pt devices by optimizing the thickness of the Al gate.

Shown in Fig. 4a is a cumulative probability plot of V_{SET} and V_{RESET} for the device from Fig. 3a. While V_{RESET} is tightly distributed about 0.25 V (standard deviation, σ, of 0.06 V, V_{SET} has a mean of −0.85 V and shows significantly more variation (σ = 0.33 V).

To examine more closely whether a CF mechanism may be involved, the median resistance of the HRS and the LRS for a series of ZTO MIM devices over a two-orders of magnitude range in area was measured and is shown in Fig. 4b. In the absence of direct experimental evidence such as TEM cross sections or AFM images of high conduction hot spots, the inverse dependence of R_{HRS} on the area combined with the relative lack of area dependence for the R_{LRS} and reduction in R_{HRS}/R_{LRS} has been interpreted as consistent with a CF model for resistive switching [8,11,26]. For example, if the LRS conduction occurs through a few dominant CFs, R_{LRS} would depend only weakly on area. The inverse area dependence observed for the HRS is consistent with bulk conduction throughout the device area (the dominant CFs are ruptured). The superlinear dependence may indicate enhanced leakage in the larger devices, possibly related to extrinsic defects.

A plot of log |current| vs. log |voltage| for a typical switching cycle of a 50 μm × 50 μm device with an operating CC of 150 μA is shown in Fig. 5a. Conduction in the LRS as well as in the HRS at low negative bias is most likely Ohmic, as indicated by the near unity slope. For the HRS at higher negative biases, just below the

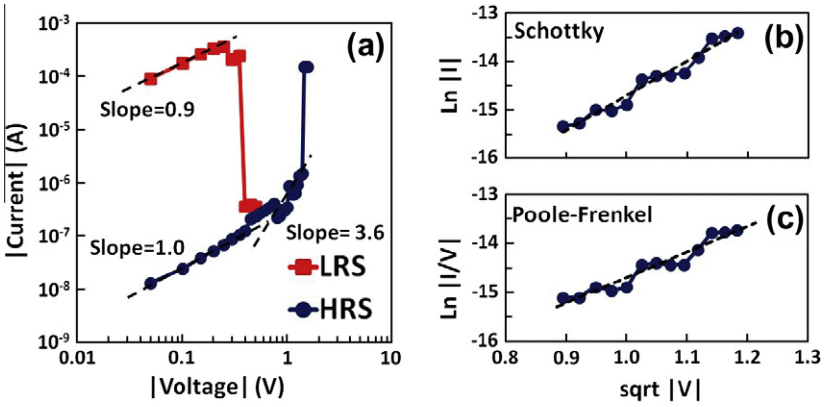

Fig. 5. (a) Plot of log |current| vs. log |voltage| for 50 μm × 50 μm using a 150 μA operating-CC along with (b) Schottky plot of ln |*I*| vs. sqrt |*V*|, and (c) a Poole–Frenkel plot of ln |*I*/*V*| vs. sqrt |*V*| for the high slope part of the HRS data.

SET operation, there is a significant increase in slope, indicating that a different conduction mechanism becomes dominant. Two possibilities are Poole–Frenkel (P–F) emission and Schottky emission. In P–F emission, the current density, *J*, is described by $J \sim Eexp\left[\frac{-q(\phi_B-\sqrt{qE/\pi\varepsilon_i})}{kT}\right]$ where *E* is the electric field, *q* is the electronic charge, φ_B is the barrier height, ε_i is the relative dielectric constant of the ZTO, *k* is Boltzmann's constant, and *T* is temperature. For Schottky emission, $J \sim A^*T^2exp\left[\frac{-q(\phi_B-\sqrt{qE/4\pi\varepsilon_i})}{kT}\right]$ where A^* is the effective Richardson constant.

Shown in Fig. 5b is a linearized P–F plot of ln |*I*/*V*| vs. sqrt |*V*| for the high slope region of the HRS data in Fig. 5a. Shown in Fig. 5c is a linearized Schottky plot of ln |*I*| vs. sqrt |*V*| for the same high slope region of the HRS data in Fig. 4a. It is seen that both P–F and Schottky emission plots of this region can be fit by straight lines. Using methods that have been published previously [27,28], we differentiate between P–F and Schottky by comparing the high frequency dielectric constant, κ_E, of ZTO to the estimated optical dielectric constants (κ_{PF} and κ_S) extracted from the straight line slopes of the respective P–F and Schottky plots. The slope, β_{PF}, of the P–F plot in Fig. 5b can be expressed as $\beta_{PF} = (q^3/4\pi\varepsilon_0\kappa_{PF}d)^{1/2}$, where *d* is the thickness of the ZTO, and ε_0 is the vacuum permittivity. Similarly, the slope, β_S, of the Schottky plot in Fig. 5c can be expressed as $\beta_{PF} = (q^3/4\pi\varepsilon_0\kappa_S d)^{1/2}$.

Examining all switching cycles, κ_{PF} was found to be between 26 to 54, whereas κ_S was found to be between 4 and 7. κ_E was estimated to be 3.24 from the square of the refractive index of ZTO, n_{ZTO} (measured via ellipsometry to be 1.8). Whereas κ_E is comparable to κ_S, it is much smaller than κ_{PF}, suggesting that P–F emission can be eliminated from consideration as the conduction mechanism for the HRS at higher negative biases. Schottky conduction is consistent with our analysis and involves emission over a barrier, suggesting a role for an interfacial barrier in these devices, analogous with studies reporting the formation of an IL at the Al/metal oxide interface [5–7,23].

Based on the atypical switching direction (negative bias for SET and positive bias for RESET (consistent with an IL at the Al/ZTO interface) [5,7,23]) the relative independence of both the GF CC and the R_{LRS} on area (consistent with, but not direct evidence for, filamentary conduction) [3,8,9,11,26], and the apparent importance of Schottky conduction during the SET operation (consistent with a role for an interfacial barrier), we can form a hypothesis for the switching mechanism in our ZTO memristive devices. During Al deposition, Al is favorably oxidized [24] by extracting oxygen ions from the underlying ZTO film, creating O-vacancies in the ZTO, forming a thin AlO_x IL at the Al/ZTO interface, and leaving the device in the HRS [5–7,22,29,30]. During the GF process, when a sufficient negative bias is applied to the top Al electrode, negatively charged oxygen ions in the AlO_x IL (or perhaps positively charged oxygen vacancies in the ZTO) drift toward the ZTO (AlO_x - IL) [4,22,23]. The migration of these native defects results in redox reactions culminating in the formation of CFs in the AlO_x IL and causing the device to SET from the HRS to the LRS. Finally, when a high enough positive bias is applied, the oxygen ions (vacancies) drift back into the AlO_x IL (ZTO), rupturing the CFs and reforming the AlO_x barrier so that the device is RESET from the LRS back to the HRS.

4. Conclusion

In conclusion, we have demonstrated BRS using solution deposited ZTO, an amorphous oxide semiconductor, as the active layer in Al/ZTO/Pt MIM crossbar devices. Although a forming step is not required, a gradual-forming process, in which the CC limiting the initial negative bias SET operation is incrementally increased until the first bipolar switching operation is observed at positive bias, greatly improved switching characteristics for these devices. ZTO devices showed switching ratios greater than 10^3, long retention times, and good endurance. Although the physical basis for switching requires further investigation, a weak area dependence of both the GF CC and the R_{LRS} is consistent with a role for CFs [3,8,9,11,26] while the switching polarity and analysis of the conduction mechanism in the HRS and LRS are consistent with a role for an interfacial layer [5,7,22,23]. Although much further work will be necessary to unravel the fundamental physics, electrical measurements of BRS in these Al gate ZTO devices appears to be consistent with a combination of CFs and interface effects (such as oxygen-driven redox reactions), with a role for oxygen ion or vacancy drift [2–7,23]. Overall, we find that ZTO shows great potential and merits further study as a low cost material for embedding low power memory with logic on TFT displays with little change in process flow.

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